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	Paper Title:	Design of Effective Noise Cancellation Circuits in Acoustic	
	<p>Abstract: This paper presents an effective noise cancellation circuit in acoustic, which is designed, simulated, and measured. The feedforward earphone is with high performance of noise suppression. The main structure consists of a controller, a notch filter, a high-pass filter, a microphone, and a speaker. The noise detection microphones pick up sounds and divide them into human voice and low-frequency noise. After passing through the gain-controlled filters, the embedded filtered-X least mean-square (FxLMS) algorithm will generate anti-noise signals with 180° phase difference to ambient noise. Consequently, these anti-noise signals will be transformed from digital formats to analog format, and thereby transformed to acoustic signal by the speakers. The generated acoustic signal will cancel the ambient noise, leading to a quiet zone. According to the measured results, it is indicated that a 15-dB noise reduction is achieved.</p> <p>Keywords: Active noise cancellation, low-frequency noise, feed forward type, feedback type.</p> <p>References:</p> <ol style="list-style-type: none"> 1. I. T. Ardekani and W. H. Abdulla, "Active noise control in three dimensions," IEEE Trans. Control Syst. Technol., 2014. (Accepted) 2. D. C. Chang and F. T. Chu, "Feedforward active noise control with a new variable tap-length and step-size filtered-X LMS algorithm," IEEE Trans. Audio, Speech, Lang. Process., vol. 22, no. 2, pp. 542-555, Feb. 2014. 3. D. C. Chang and F. T. Chu, "A new variable tap-length and step-size FxLMS algorithm" IEEE Signal Process. Lett., vol. 22, no. 2, pp. 542-555, Feb. 2014. 4. M. Guldenschuh and R. D. Callafon, "Detection of secondary-path irregularities in active noise control headphones," IEEE Trans. Audio, Speech, Lang. Process., vol. 22, no. 7, pp. 1148-1157, July 2014. 5. S. Ahmed, M. T. Akhtar, and X. Zhang, "Online acoustic feedback mitigation with improved noise-reduction performance in active noise control systems," IET Signal Processing, vol. 7, Iss. 6, pp. 505-514, Aug. 2013. 6. http://www.ams.com. 		1-3
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	Paper Title:	High Performance Current-Mode Multiplier Circuit based on Carbon Nanotube Transistors	
	<p>Abstract: Carbon Nanotube Field Effect Transistor (CNFET) is a promising new technology that overcomes several limitations of traditional silicon integrated circuit technology. In recent years, the potential of CNFET for analog circuit applications has been explored. This paper proposes a novel four quadrant analog multiplier design using CNFETs. The simulation based on CNFET technology shows that the proposed multiplier has better features than CMOS Multiplier. Multiplier-divider circuits is using in digital signal processing base on neural networks and communications (amplifiers with variable gain, modulators, detectors and,...).In Most of CMOS analog circuit, transistors are only in triode or saturate regions; till now both regions not used. In this one kind of current mode multiplier-divider circuits is intrudused.it is very simple, has low die area and wide range in low voltage. All tough this circuit has no sense to temperature variation and varying parameters.</p> <p>Keywords: CNT, Analog signal processing, current- mode operation, multiplier, reconfigurable circuits.</p> <p>References:</p> <ol style="list-style-type: none"> 1. R. Harjani, "A low-power CMOS VGA for 50 Mb/s disk drive read channels," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process, vol. 42, no. 6, pp. 370-376, Jun. 1995. 2. A. Motamed, C. Hwang, and M. Ismail, "A low-voltage low-power wide rang CMOS variable gain amplifier," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process, vol. 45, no. 7, pp. 800-811, Jul. 1998. 3. C. Popa, Synthesis of Computational Structures for Analog Signal Processing, New York, USA: Springer-Verlag, 2011. 4. C. Popa, Superior-Order Curvature-Correction Techniques for Voltage References, New York, USA: Springer-Verlag, 2009. 5. C. Popa, "Low-power CMOS bulk-driven weak-inversion accurate current-mode multiplier/divider circuits," in Proc. Int. Conf. Electr Electron. Eng., 2003, pp. 66-73. 6. C. Popa, "Computational circuits using bulk-driven MOS devices," in Proc. IEEE EUROCON Conf., May 2009, pp. 246-251. 7. C. Popa, "Logarithmic curvature-corrected weak inversion CMOS voltage reference with improved performances," presented at the 11th Int. Workshop on Thermal Investigations on ICs and Systems, Lake Maggiore, Italy, 2005. 8. C. Popa, "A new curvature-corrected voltage reference based on the weight difference of gate-source voltages for subthreshold-operated MOS transistors," in Proc. Int. Symp. Circuits Syst., 2003, pp. 585-588. 9. C. C. Chang and S. I. Liu, "Weak inversion four-quadrant multiplier and two-quadrant divider," Electron. Lett., vol. 34, no. 22, pp. 2079-2080, Oct. 1998. 10. M. Gravati, M. Valle, G. Ferri, N. Guerrini, and N. Reyes, "A novel current-mode very low power analog CMOS four quadrant multiplier," in Proc. 31st Eur. Solid-State Circuits Conf., Sep. 2005, pp. 495-498. 11. C. Popa, "High accuracy CMOS multifunctional structure for analog signal processing," in Proc. Int. Semicond. Conf., 2009, pp. 427-430. 12. C. Popa, "CMOS multifunctional computational structure with improved performances," in Proc. 33th Ed. Annu. Semicond. Conf., vol. 2. 2010, pp. 471-474. 13. C. Popa, "Multiplier circuit with improved linearity using FGMOS transistors," in Proc. Int. Symp. ELMAR 2009, pp. 159-162. 14. Y. H. Kim and S. B. Park, "Four-quadrant CMOS analogue multiplier," Electron. Lett., vol. 28, no. 7, pp. 649-650, Mar. 		4-7

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